Amendments to the Claims:

1. (Currently Amended) An integrated circuit capacitor, comprising:

a first capacitor electrode on a semiconductor substrate, said first capacitor electrode comprising a conductive layer pattern ~~recrystallized amorphous silicon layer~~ having a first concentration of first conductivity type dopants therein, and a hemispherical grain (HSG) silicon surface layer on the conductive layer pattern, ~~recrystallized amorphous silicon layer,~~ said HSG silicon surface layer having a second concentration of first conductivity type dopants therein which is greater than the first concentration;

~~a diffusion barrier layer on the HSG silicon surface layer;~~

a dielectric layer on the HSG silicon surface layer ~~diffusion barrier layer~~; and

a second capacitor electrode on the dielectric layer.

2. (Currently Amended) The integrated circuit capacitor of Claim 5~~1~~, wherein the diffusion barrier layer comprises a silicon nitride layer having first conductivity type dopants therein; and wherein the dielectric layer comprises tantalum oxide.

3. (Original) The integrated circuit capacitor of Claim 2, wherein the silicon nitride layer comprises a composite of a first silicon nitride layer formed by rapid thermal nitridation (RTN) and a second silicon nitride layer formed by chemical vapor deposition (CVD).

4. (Original) The integrated circuit capacitor of Claim 2, wherein the tantalum oxide layer comprises a composite of a plurality of densified tantalum oxide layers.

5. (New) The integrated circuit capacitor of Claim 1, further comprising a diffusion barrier layer between the HSG silicon surface layer and the dielectric layer.

6. (New) The integrated circuit capacitor of Claim 5, wherein the diffusion barrier layer comprises silicon nitride.

7. (New) The integrated circuit capacitor of Claim 5, wherein the diffusion barrier layer comprises first conductivity type dopants.

8. (New) The integrated circuit capacitor of Claim 5, wherein the diffusion barrier layer has a thickness between about 5 Å and 100 Å

9. (New) The integrated circuit capacitor of Claim 1, wherein:

the first concentration of first conductivity type dopants is less than about $1x10^{20}$ cm^{-3}; and

the second concentration of first conductivity type dopants is greater than about $1x10^{20}$ cm^{-3}.

10. (New) The integrated circuit capacitor of Claim 1, wherein the conductive layer patter comprises amorphous silicon.

11. (New) The integrated circuit capacitor of Claim 1, wherein the conductive layer pattern comprises polycrystalline silicon.

12. (New) The integrated circuit capacitor of Claim 1, wherein the conductive layer pattern comprises:

a polycrystalline silicon layer in contact with the semiconductor substrate; and

an amorphous silicon layer on the polycrystalline silicon layer.

13. (New) The integrated circuit capacitor of Claim 1, wherein the dielectric layer comprises a nitride-oxide (NO) layer having a thickness in a range between about 40 and 70A.

14. (New) The integrated circuit capacitor of Claim 1, wherein the dielectric layer comprises tantalum oxide (Ta_2O_5).